

## WEST Search History





DATE: Wednesday, October 04, 2006

<u>Hide?</u>	<u>Set Name</u>	<u>Query</u>	<u>Hit Count</u>
		<i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L44	L43 not l42	1
<input type="checkbox"/>	L43	fork and l39	3
<input type="checkbox"/>	L42	l13 and l39	11
<input type="checkbox"/>	L41	l12 and l39	0
<input type="checkbox"/>	L40	l26 and L39	0
<input type="checkbox"/>	L39	712/239.ccls.	465
<input type="checkbox"/>	L38	compiler with L31	2
<input type="checkbox"/>	L37	identif\$3 with L31	1
<input type="checkbox"/>	L36	recogniz\$3 with L31	1
<input type="checkbox"/>	L35	test\$3 with L31	2
<input type="checkbox"/>	L34	illegal instruction\$1 with test\$3	25
<input type="checkbox"/>	L33	unsupported with instruction\$1 with test\$3	0
<input type="checkbox"/>	L32	test\$3 with L31	2
<input type="checkbox"/>	L31	unsupported feature\$1	97
<input type="checkbox"/>	L30	unsupported feature\$1\$1	97
<input type="checkbox"/>	L29	unsupported instruction\$1	11
<input type="checkbox"/>	L28	illegal instruction\$1	589
<input type="checkbox"/>	L27	instruction with L26	20
<input type="checkbox"/>	L26	test\$3 with processor with capabilit\$3	382
<input type="checkbox"/>	L25	compiler with L12	1
<input type="checkbox"/>	L24	L12 with instruction\$1	36
<input type="checkbox"/>	L23	intel.asn. and L12	16
<input type="checkbox"/>	L22	L14 and L12	0
<input type="checkbox"/>	L21	(audio same chipset) and L17	11
<input type="checkbox"/>	L20	(audio and chipset) and L18	4
<input type="checkbox"/>	L19	(audio same chipset) and L18	0
<input type="checkbox"/>	L18	intel.asn. and L17	8
<input type="checkbox"/>	L17	input-output with chipset	115
<input type="checkbox"/>	L16	join and L14	7
<input type="checkbox"/>	L15	join same L14	2
<input type="checkbox"/>	L14	fork with L13	27

<input type="checkbox"/>	L13	thread\$1 with speculat\$3	317
<input type="checkbox"/>	L12	detect\$3 with processor with capabilit\$3	742
<input type="checkbox"/>	L11	(mch) and intel.as	0
<input type="checkbox"/>	L10	(memory controller hub) and intel.as	0
<input type="checkbox"/>	L9	intelligent hub and intel.as	0
<input type="checkbox"/>	L8	intelligent hub and intel.as	0
<input type="checkbox"/>	L7	intel.as. and L6	36
<input type="checkbox"/>	L6	system bus same memory controller same bus bridge	1757
<input type="checkbox"/>	L5	intel.as. and L4	61
<input type="checkbox"/>	L4	processors with L3	259
<input type="checkbox"/>	L3	front side bus	1177
<input type="checkbox"/>	L2	processors with L1	5
<input type="checkbox"/>	L1	north with south with bridge with bus	640

END OF SEARCH HISTORY